Monade X paint.NET | PixelART

Cache placement policies - Wikipedia

direct-mapped, two-way, or four-way set-associative.

index for way 0 is direct, as above, but the index for way 1 is formed with a hash function.

Consider 16 kilobytes RAM, which is organized as 4-byte blocks, and a 2-way set-associative cache of 256 bytes with a block size of 4 bytes.
Because the main memory is 16kB, we need a minimum of 14 bits to uniquely represent a memory address.
Since each cache block is of size 4 bytes and is 2-way set-associative, the total number of sets in the cache is 256/(4 * 2), which equals 32 sets.

- Offset corresponds to the bits used to determine the byte to be accessed from the cache line. Because the cache lines are 4 bytes long, there are 2 offset bits.
- Index corresponds to bits used to determine the set of the Cache. There are 32 sets in the cache, and because 2^5 = 32, there are 5 index bits.
- Tag corresponds to the remaining bits. This means there are 14 – (5+2) = 7 bits, which are stored in tag field to match the address on cache request.

Pentium (original) - Wikipedia

Smart Response Technology - Wikipedia

Multi-level cell - Wikipedia

Floating-gate MOSFET - Wikipedia

Error correction code - Wikipedia

Block codes work on fixed-size blocks (packets) of bits or symbols of predetermined size. Practical block codes can generally be hard-decoded in polynomial time to their block length.

Convolutional codes work on bit or symbol streams of arbitrary length. They are most often soft decoded with the Viterbi algorithm, though other algorithms are sometimes used.

Hamming ECC is commonly used to correct NAND flash memory errors. This provides single-bit error correction and 2-bit error detection. they only suitable for more reliable single-level cell (SLC) NAND. Denser multi-level cell (MLC) NAND may use multi-bit correcting ECC such as BCH or Reed–Solomon. NOR Flash does not use any error correction.

- Hemming distance
- Levenshtein distance

The key innovation of turbo codes is how they use the likelihood data to reconcile differences between the two decoders

This iterative process continues until the two decoders come up with the same hypothesis, typically in 15 to 18 cycles.

Concatenated error correction code - Wikipedia

Low-density parity-check code - Wikipedia

Turbo code - Wikipedia

IT++ - Wikipedia

The EDC/ECC technique uses an error-detecting code (EDC) in the level 1 cache. If an error is detected, data is recovered from ECC-protected level 2 cache. The ECC/ECC technique uses an ECC-protected level 1 cache and an ECC-protected level 2 cache. CPUs that use the EDC/ECC technique always write-through all STOREs to the level 2 cache, so that when an error is detected during a read from the level 1 data cache, a copy of that data can be recovered from the level 2 cache.

Error correction code memory (ECC memory)

While 72-bit word with 64 data bits and 8 checking bits are common, ECC is also used with smaller and larger sizes

SECDED:: Binary Hamming Codes

First used of a TLB and of TIME-Sharing with the IBM 3.60/67 from the late 1960th

- Simplex configurations can include 7 I/O channels, while duplex configurations can include 14 I/O channels
- Two new program interruptions: Segment translation exception (16) and page translation exception (17)
- HR Interval Timer with 13 microseconds

ECC memory - Wikipedia

Hamming code - Wikipedia

CPU cache - Wikipedia

IBM System/360 Model 67 - Wikipedia

TSS (operating system) - Wikipedia

The IBM Time Sharing System TSS/360 is a discontinued early time-sharing operating system designed exclusively for a special model of the System/360 line of mainframes, the Model 67-2.

TSS provides users a command-line interface. Operands can be either positional or keyword, with the format "keyword=value".

System commands are divided into seven categories;

- Task management – LOGON, LOGOFF, ABEND, etc.
- Data management – CATALOG, DDEF, DELETE, etc.
- Program management – LOAD, DUMP, DISPLAY, TRAP, etc
- Command creation – PROCDEF, BUILTIN
- Message handling
- User profile – SYNONYM, DEFAULT, PROFILE, etc
- Program product language interface – ASM (Assembler (F)), COBOL, HASM (Assembler (H)), PLI (PL/I (F)), PLIOPT (PL/I Optimizing Compiler), FTNH (FORTRAN (H)), etc.

TSS/8

The operating system ran on the 12-bit PDP-8 computer and was released in 1968.

Motorola 68060 - Wikipedia

Leseprobe »Warum deine Freunde mehr Freunde haben als du« - Spektrum der Wissenschaft

TSS/8 - Wikipedia

Time-sharing system evolution - Wikipedia

IBM System/370 - Wikipedia

I / O evolutions

The block multiplexer channel, previously available only on the 360/85 and 360/195, was a standard part of the architecture. For compatibility it could operate as a selector channel. channels were available in

- single byte (1.5 MB/s) and
- double byte (3.0 MB/s) versions.

USB / BLUETOOTH 2.1 / 3,0 Lissbon-Seattle

InterNet

System/370-XA introduced a channel subsystem that performed I/O queuing previously done by the operating system.

BACKBONE

The System/390 introduced the ESCON channel, an optical fiber, half-duplex, serial channel with a maximum distance of 43 kilometers. Originally operating at 10 Mbyte/s, it was subsequently increased to 17 Mbyte/s.

SubSequently

- FIbre CONnection (FICON)
- Fibre Channel Protocol (FCP)

infrastructure and protocol onto standard FC services and infrastructure at data rates up to

16 Gigabits/sec at distances up to 100 km.

z/Architecture - Wikipedia

Alpha 21264 - Wikipedia

Alpha 21464 - Wikipedia

Compaq - Wikipedia

Extended Industry Standard Architecture - Wikipedia

The Gang of Nine was the informal name given to the consortium of personal computer manufacturing companies that together created the EISA bus. Rival members generally acknowledged Compaq's leadership, with one stating in 1989 that within the Gang of Nine "when you have 10 people sit down before a table to write a letter to the president, someone has to write the letter. Compaq is sitting down at the typewriter"

- AST Research
- Compaq Computer Corporation
- Seiko Epson Corp.
- Hewlett-Packard
- NEC Corp.
- Olivetti
- Tandy Corp.
- WYSE
- Zenith Data Systems

In 1988 - Extendet -ISA (industrie Standart Assosiation)
Hardware RAID- 32bit BUS (compatible with 8 & 16Bit ISA) - 98 bis 100 PINs | 5v/12v - 8.33Mhz Clock with dataRate by 4BYTEs (Half-dublex) about 33MB/s, but useable about 20MB/s - in a Parallel style!

1993 (Compaq ProLiant); 2003 (HP ProLiant)

The development of Micro Channel was driven by both technical and business pressures.

Compaq SystemPro - Wikipedia

ProLiant - Wikipedia

Micro Channel architecture - Wikipedia

List of interface bit rates - Wikipedia

The Micro-Channel Architekture in IBM products, (by 1987) it superseded the ISA bus and was itself subsequently superseded by the PCI bus architecture (by 1993).

It is the first draft, for the USB DEVICE und SD Connectd Mobile Architecture.

DATA over Cable[Service Interface Specification]

- 1.0 38/9Mbit/s 1997
- 2.0 38/27Mbit/s 2002
- 3.1 10/2Gbits/s 2013
- 4.0 10/6Gbits/s 2017

The Precision Time Protocol (PTP) is a protocol used to synchronize clocks throughout a computer network. On a local area network, it achieves clock accuracy in the sub-microsecond range, making it suitable for measurement and control systems. PTP is currently employed to synchronize financial transactions, mobile phone tower transmissions, GPS

The original version of PTP, IEEE 1588-2002, was published in 2002. IEEE 1588-2008, also known as PTP Version 2 is not backward compatible with the original 2002 version.

IEEE 802.1AS is an adaptation of PTP for use with Audio Video Bridging and Time-Sensitive Networking.

HyperTransport - Wikipedia

RapidIO - Wikipedia

Precision Time Protocol - Wikipedia

Audio Video Bridging - Wikipedia

A domain[i] is an interacting set of clocks that synchronize to one another using PTP. Clocks are assigned to a domain by virtue of the contents of the Subdomain name (IEEE 1588-2002) or the domainNumber (IEEE 1588-2008) fields in PTP messages they receive or generate. Domains allow multiple clock distribution systems to share the same communications medium.

The best master clock (BMC) algorithm performs a distributed selection of the best candidate clock based on the following clock properties:
Identifier – A universally unique numeric identifier for the clock. This is typically constructed based on a device's MAC address.

PTP V2 (IEEE 1588-2008) defines the overall quality of a clock by using the data fields clockAccuracy and clockClass.

IEEE 1588-2002 used a single boolean variable to indicate precedence. IEEE 1588-2008 features two 8-bit priority fields.

Variance – A clock's estimate of its stability based on observation of its performance against the PTP reference.

Wayback Machine

MT6235 GSM/GPRS Baseband Processor Data Sheet Revision 1.02 (7. April 2008)
it has a ARM926EJ-S, supporting the ARMv5TE instruction set and featuring a full MMU. This means that the MT6235 is capable of running a regular Linux kernel, as soon as somebody has implemented the device drivers for the SoC internal peripherals.

MT6260 is a feature-rich and extremely powerful single-chip solution for high-end GSM/GPRS and EDGE-Rx capability. Based on the 32-bit ARM7EJ-STM RISC it has 1 cores, 1 threads, a maximum frequency of 0,4GHz. 28nm, (8KB Catch - max Memory of 128MB, 364 Mhz, 8 MB RAM, GSM. Bluetooth. LCD controller. PWM. USB and dozens more.

???Release date: q2 2017??? 2013 / 2015?6261

- A highly integrated Bluetooth transceiver which is fully compliant with Bluetooth specification v3.0
- FM receiver supporting both audio broadcast de-modulation and RDS/RBDS data decoding.
- Supports LCD module with maximum resolution up to 480x320
- display memories with up to 4 blending layers

MT6235 DSP - OsmocomBB - Open Source Mobile Communications

MT6260A pdf, MT6260A description, MT6260A datasheets, MT6260A view ::: ALLDATASHEET :::

Reverse-Engineering A Superior Chinese Product | Hackaday

From Gongkai to Open Source « bunnie's blog

Schedule 31. Chaos Communication Congress

Computer data storage - Wikipedia

QNX Download Center

ILI9341 LCD Controller – ECE353: Introduction to Microprocessor Systems – UW–Madison

Server Message Block - Wikipedia

Barry Feigenbaum originally designed SMB at IBM in early 1983 with the aim of turning DOS INT 21h local file access into a networked file system.[9] Microsoft has made considerable modifications to the most commonly used version. Microsoft merged the SMB protocol with the LAN Manager product which it had started developing for OS/2 with 3Com around 1990, and continued to add features to the protocol in Windows for Workgroups (c. 1992) and in later versions of Windows.

Other improvements include caching of file properties, improved message signing with HMAC SHA-256 hashing algorithm and better scalability by increasing the number of users, shares and open files per server among others. The SMB1 protocol uses 16-bit data sizes, which amongst other things, limits the maximum block size to 64K. SMB2 uses 32- or 64-bit wide storage fields, and 128 bits in the case of file-handles, thereby removing previous constraints on block sizes...

File descriptor - Wikipedia

Handle (computing) - Wikipedia

Callback (computer programming) - Wikipedia

Job control (Unix) - Wikipedia

- Job control is a facility developed to make this possible, by allowing the user to start processes in the background, send already running processes into the background, bring background processes into the foreground, and suspend or terminate processes.
- The concept of a job maps the (shell) concept of a single shell command to the (operating system) concept of the possibly many processes that the command entails. Multi-process tasks come about because processes may create additional child processes, and a single shell command may consist of a pipeline of multiple communicating processes. For example, a command to select lines containing the text "title", sort these alphabetically, and display the result in a pager.

In computer programming, a handle is an abstract reference to a resource that is used when application software references blocks of memory or objects that are managed by another system like a database or an operating system.

Terminal pager - Wikipedia

There are two types of callbacks, differing in how they control data flow at runtime: blocking callbacks (*synchronous* callbacks) and deferred callbacks (*asynchronous* callbacks).

- While blocking callbacks are invoked before a function returns
- deferred callbacks may be invoked after a function returns. Deferred callbacks are often used in the context of I/O operations or event handling, and are called by interrupts or by a different thread in case of multiple threads.

On Linux, the set of file descriptors open in a process can be accessed under the path /proc/PID/fd/, where *PID is the process identifier.*

- *Sockets are created only during the lifetime of a process of an application running in the node.*

The term socket is also used for the software endpoint of node-internal inter-process communication (IPC), which often uses the same API as a network socket.

An IPC mechanism Synchronization primitives may be used to have synchronous behavior with an asynchronous IPC mechanism.

Network socket - Wikipedia

Inter-process communication - Wikipedia

9P (protocol) - Wikipedia

RISC OS

Between 1987 and 1998, RISC OS was included in every ARM-based Acorn computer mode

NCOS is the graphical user interface-based operating system developed for use in Oracle Corporation's Network Computers, which are discontinued. It was adapted by Acorn Computers from its own RISC OS, which was originally developed for their range of Archimedes desktop computers. It shares with RISC OS the same 4 MB ROM size and suitability for use with TV displays.

The 3D-Interaktiv-Character Set

- S30+
- C:\>2*30
- =60*6400
- =384000/4
- (480/2)*320>(1/2)+(4/2)=>+/-3
- 4MB/3=1,25M*N=>1,98xy<=Z
- Z:\>720-1022bit *(diff:222BIT)*

(NOKIA -C*-OS)

At 0x83 is a box with another box inside it on the top left-hand corner, meaning "resize window". At 0x84 is a 'bubble-writing' X, meaning "close window". At 0x87 is an unusual character that is a subscript 8 followed by a superscript 7. It is not proposed for Unicode. At 0x88, 0x89, 0x8A, and 0x8B are left, right, up, and down bubble arrows for window scrollbars

RISC OS - Wikipedia

NCOS - Wikipedia

RISC OS character set - Wikipedia

www.riscos.com - Main Index

Die 44PIN bzw. 28PIN einer MCU lassen sich dementsprechend solide Verteilen.

- 44 halbe a 22... dabei ist aber auch in/out zuberücksichtigen
- 44-1... 43=42+1 ... 1=1/2=0v1 somit 21+0 und 21-1 = FTP
- kommunikation über Kabel = PORT 8080 = 4bit * 20bit + 1 = http
- Bei 28PIN ist es eine absolute SingleCore welches nur noch 27+1 bzw. 27-0 Faktorisiert

Auf dieser Technik aufbauend, lassen sich in Moderneren Chips auch Anschlü mit 78 94 oder 129 PINS Konzeptionelle verbauen. Die leistung wird hierbei dem Messagingkonzept angepasst und ein Internes - Prozessmanagement für die Datenkommunikation auf der Ebedded-Ebene realisiert.

Das Nokia OS [s(3)0+] verwendet 35PIN
5Pin für 3x5bit im Kern (perCycle)
30PIN 2*30=60
bzw. 15in kern, 15 im catch
bei 60/4=15

S(3)0=> 3x15=45-5=40bit
0=Layer OS (Statisch)
(3)=der A10 StackPointer
S=Die Klasse S' zur Makulatur
REST: 15-20=>2*8 oder 2*10
REST=2xUART

Bridge (Netzwerk) – Wikipedia

Advanced High-performance Bus – Wikipedia

Advanced Microcontroller Bus Architecture – Wikipedia

ARM926EJ-S Development Chip Reference Manual

Field Programmable Gate Array – Wikipedia

Motorola 88000er-Familie – Wikipedia

Freescale ColdFire – Wikipedia

Quad Integrated Communication Controller (QUICC) | NXP Semiconductors

The NOKIA OS base line...

- vom Motorola 68060 wrt (88k)
- zum MediaTek 6260 (6261)
- Under the Hood from NXP 68(3)60 (s(3)0+

Quad Integrated Communikation Controller
RISC Controller with 14 Serial DAMS and 7Channels but a 2.5Kbyte DualPORT RAM and 4PurposeTimer in general also 2 IDMAs in the CPU32+ core and many many more features

- dynamic 32bit data bus (8 and 16 bits) +32 address lines
- static design (0-33mhz) pro operation
  366mhz/33 11,09 also ca. 367mhz
  357/5=73,4/3=24,xyz (1000*24bit/Sek)
  ander rum, bei 50herz bleiben 2350herz über!
- Memory Controler (8 Banks)
- interface for DIMM-DDR, SDRAM
- EPROM Flash etc.
- Bootchip select 3-16 or 32bit memory
- 4pTimer : 4x16bit or 2x32bit
- 2xIndependent DMA
- continuos mode transmission and reception on all 7 serial channels
- 4x Baud (9600) rate generators
- 4 SCCs (UART Sinc/Asyn) HDLS Bus for PPP
  IEEE802.3 1-2(25mhz) or 1-3(33mhz)
- Parallel Interface Port between QUICC
- 2x SMCs

The QUICC can be described as a next-generation MC6 8 | 30*2 ein syllogismus

Quad Integrated Communication Controller (QUICC) | NXP Semiconductors

The Buggles - Video Killed The Radio Star (Official Music Video)

Z:\>SD HD (32GB) | 720-1022 (222)

It particularly excels in communications activities. The QUICC (pro nounced "quick") can be described as a next-generation MC68302 with higher performance in all areas of device operation, increased flexibility, major extensions in capability, and higher integration. The term "quad" comes from the fact that there are four serial communi cations controllers (SCCs) on the device; however, there are actually seven serial channels: four SCCs, two serial management controllers (SMCs), and one serial peripheral interface (SPI)

- Ideal for E1/T1 applications, the QMC protocol can multiplex any 64-channel combination of subgroups to one TDM interface.
- The SCC only performs the parallel-to-serial conversion and adds elasticity through its FIFO memory.

The (BUS) HDLC mode register (PSMR) have two additional defined bits. The width and the location of the register has not changed.

- 0=10 bits
- 1=9 bits

Priority Mode, needed to be counted prior to frame

MC68360B.pdf

MC68360UM.pdf

HD Bus vs TRIS Pin

Bit 1 BMC | HDLC BUS Collusion Sense Mode
the *sample point of collision detection*

- 0 = collision is sensed after 1/2 bit delay (or at3/4 bit delay if the clock duty *cycle is 25%).*
- 1 = collision is sensed after one bit delay

Bit 0 FDE (Full Duplex Ethernet) This bit when set enables full duplex Ethernet operation.

- 0 = Disable full duplex ethernet.
- 1 = Enable full duplex ethernet.

The **RISC revision** number in the **XC**68360 at address (MiscBase+$00) has the value $0002. Revision **A0 device** has a mask number **0C63T**, and revision **A1** has a mask number **1C63T**. Both revisions **A0 and A1** have microcode revision number of **$0001**

TRIS Pin did not tristate clock out pins **(CLK01 and CKL02)**

Interfacing the MC68060 to MC68360

AN2031 Interfacing the 68360 QUICC to T1/E1 Systems

T-Systems T1/E1

e1=2048Mbps by 30 No. of Vois Channels
e2=8448Mbps by 120...
e3=480Mbps

US Digital Signal No, (DS 1/1C/2/2/3/4)
T1/c/g (T-D1)

- DS1 1544 by 24
  DS1C 3152 by 48
  DS2 G 6443 by 96
- DS2/T2 6312 by 96

about TRIS Pin => (T-D2)
DS3 / T3 44736 by 672
DS4 / T4 274176 by 4032

40 | 32 => 4032 rest 54
in einer 10x10 Matrix
=154= Xc:\> (Tsystem) </:Z= HD (eplus)

(T4]e1e2e3[O2) | used by ReFS (SCC 1-2-3-4)

- CLKa= CLK1-2-3-4
- CLKb= CLK5-6-7-8

working on the seven Channels by 8 BANKs
the CLK8 Pin - is routed through the banks of clocks every CLK is used to Receive!

by 25Mhz 2 SCC with 1Mbps fulldublex in ethernet Mode. by 33Mhr 3 SCC could be used

1 SCC is on one Pin spezial for the SIA serial interface adapter! the rest of the 7th are used for 2 or 3 SCCs singel half dublex or full

2:1 +(1) or 3 +(1) Transmission or Receive have to seperatet use of the SCCs / CLKs!

- TXD pin transmit Data
- RXD receive Datat

ethernet/IEEE802.3 Handbook from AMD about the 10BASE-2 or 10BASE-T

QUICC Ethernet Address Filtering with DSP56002

Profibus – Wikipedia

How Apple Just Changed the Entire Industry (M1 Chip)

Latch – Wikipedia

Wenn man den Begriff als Verb latchen verwendet, meint man damit oft ein Fehlverhalten einer digitalen Hardwareschaltung. Sie bleibt in einem bestimmten Zustand stecken („dieser Zustand wird gelatcht“), obwohl die Eingangssignale eigentlich eine Änderung des Ausgangszustands erfordern. Ursache für solches Festhängen kann Überlastung einzelner Schaltungsteile sein, eine Race Condition oder auch thermischer Einfluss.

How Imaginary Numbers Were Invented

Math Has a Fatal Flaw

Niels Henrik Abel – Wikipedia

es gibt gefühlt unendlich viele Protokolle, doch am end vom TAG, wird jedes auf dem SOCKEt Definiert! Siehe ProfiBUS usw.

next Steps:

- Coffee Lecture
- Mathematik im Kontext moderner Informtionswissenschaft und Infrastruktur
  (MiMiMi)
- Time Keeping

part0-titlepage.jnt

GitHub - dotnet/csharp-notebooks: Get started learning C# with C# notebooks powered by .NET Interactive and VS Code.

OntologySummit - OntologPSMW

Prince of Persia (1992 Macintosh) Complete Playthrough - Old Macintosh Game - Bing video

"Aang vs. Ozai" FULL FINAL BATTLE 🔥 Avatar: The Last Airbender - Bing video

Windows PowerShell Inventor Jeffrey Snover Interview by Evrone

pixel per inch - Bing

Punktdichte – Wikipedia

Über den Verlag - Westend Verlag GmbH

Hurenkind und Schusterjunge – Wikipedia

Mathematik – Wikipedia

Fermat-Zahl – Wikipedia

From Hilbert's 13th problem to essential dimension and back

The Most Famous Paradox in Physics Nears Its End | Quanta Magazine

Windows PowerShell Inventor Jeffrey Snover Interview by Evrone

jeffrey snover - Bing

Monads

The Assassin Puzzle | Infinite Series

Dolby – Wikipedia